

**AMENDMENTS TO THE CLAIMS**

Claims 1-28. (Canceled)

29. (Currently Amended) A semiconductor device comprising:

a substrate;

an insulating layer provided over said substrate; and

an electropolished patterned metal layer provided ~~[[over]]~~ within an opening of said insulating layer, wherein said electropolished metal layer has a thickness of approximately 50 to 300 Angstroms and wherein a top surface of said electropolished metal layer is electropolished down to said insulating layer so that said top surface of said electropolished metal layer is ~~below or~~ at the same level with a top surface of said insulating layer.

30. (Original) The semiconductor device of claim 29, wherein said electropolished patterned metal layer contains a material selected from the group consisting of noble metals, noble metal alloys and noble metal oxides.

31. (Original) The semiconductor device of claim 29, wherein said electropolished patterned metal layer contains a noble metal.

32. (Original) The semiconductor device of claim 31, wherein said electropolished patterned metal layer is a platinum layer.

Claim 33. (Canceled)

34. (Previously presented) The semiconductor device of claim 29, wherein said electropolished patterned metal layer has a thickness of approximately 100 Angstroms.

35. (Original) The semiconductor device of claim 29, wherein said electropolished patterned metal layer forms a lower capacitor electrode of said semiconductor device.

36. (Currently amended) A memory cell comprising:

~~an electropolished patterned metal layer provided over a substrate, said electropolished patterned metal layer having a thickness of approximately 50 to 300 Angstroms;~~

a transistor including a gate fabricated on ~~[[said]]~~ a semiconductor substrate and including a source/drain region in said semiconductor substrate disposed adjacent to said gate;

an electropolished metal layer within an insulating layer provided over said substrate; and

a container capacitor including a lower electrode and a dielectric layer over said lower electrode, said lower electrode having a surface aligned over said source/drain region, said electropolished patterned metal layer forming said lower electrode, and said dielectric layer being in contact with said insulating layer.

37. (Original) The memory cell of claim 36, wherein said electropolished patterned metal layer contains a material selected from the group consisting of noble metals, noble metal alloys and noble metal oxides.

38. (Original) The memory cell of claim 37, wherein said electropolished patterned metal layer contains a noble metal.

39. (Original) The memory cell of claim 38, wherein said electropolished patterned metal layer is a platinum layer.

Claim 40. (Canceled)

41. (Previously presented) The memory cell of claim 36, wherein said electropolished patterned metal layer has a thickness of approximately 100 Angstroms.

Claim 42. (Canceled)

Claim 43. (Canceled)

44. (Currently Amended) A processor-based system comprising:

a processor; and

an integrated circuit coupled to said processor, at least one of said integrated circuit and processor comprising a container capacitor provided within an insulating layer, said container capacitor including a lower electrode, said lower electrode comprising an electropolished patterned metal layer having a thickness of approximately 50 to 300 Angstroms, wherein a top surface of said electropolished patterned metal layer is ~~below or~~ at the same level with a top surface of said insulating layer.

45. (Original) The processor-based system of claim 44, wherein said electropolished patterned metal layer contains a material selected from the group consisting of noble metals, noble metal alloys and noble metal oxides.

46. (Original) The processor-based system of claim 45, wherein said electropolished patterned metal layer contains a noble metal.

47. (Original) The processor-based system of claim 46, wherein said electropolished patterned metal layer is a platinum layer.

Claim 48. (Canceled)

49. (Original) The processor-based system of claim 44, wherein said electropolished patterned metal layer has a thickness of approximately 100 Angstroms.

Claim 50. (Canceled)

51. (Original) The processor-based system of claim 44, wherein said integrated circuit is a memory module.

52. (Original) The processor-based system of claim 51, wherein said memory module is a DRAM memory.

53. (Original) The processor-based system of claim 51, wherein said memory module is a SRAM memory.

54. (Original) The processor-based system of claim 51, wherein said memory module is a MCM memory.

55. (Previously presented) A container capacitor comprising:

a lower electrode provided within a first insulating layer, said lower electrode comprising an electropolished patterned metal layer having a bottom wall and vertical sidewalls extending upwardly therefrom;

a second insulating layer provided over said electropolished patterned metal layer and in contact with said first insulating layer; and

an upper electrode provided over said second insulating layer.

56. (Previously presented) The container capacitor of claim 55, wherein said electropolished patterned metal layer contains a material selected from the group consisting of noble metals, noble metal alloys and noble metal oxides.

57. (Previously presented) The container capacitor of claim 55, wherein said electropolished patterned metal layer has a thickness of approximately 50 to 300 Angstroms.

58. (Previously presented) The container capacitor of claim 55, wherein said electropolished patterned metal layer has a thickness of approximately 100 Angstroms.

59. (Previously presented) A container capacitor provided within an opening of an insulating layer of a substrate comprising:

a barrier conductive layer provided at a bottom of said opening;

a lower electrode provided over said barrier conductive layer, said lower electrode comprising an electropolished patterned metal layer having a bottom and vertical sidewalls extending upwardly from said bottom, said lower electrode having a thickness of approximately 100 Angstroms;

a dielectric material provided over said electropolished patterned metal layer and in contact with said insulating layer; and

an upper electrode provided over said dielectric material and wherein said lower electrode, said dielectric material and said upper electrode form a container capacitor.

60. (Currently amended) A container capacitor structure comprising:

an insulating layer provided over a substrate;

a plurality of openings provided in said insulating layer; [[and]]

a plurality of lower capacitor electrodes provided along the bottom and sidewalls of respective ones of said openings, said lower electrodes being formed as discrete electropolished metal layers; and

a dielectric layer associated with each of said discrete lower electrodes, said dielectric layer being in contact with said insulating layer.

61. (Currently amended) The capacitor structure of claim 60, wherein said capacitor structure further comprises ~~a dielectric layer and~~ an upper electrode associated with each of said discrete lower electrodes.

62. (Previously presented) The capacitor structure of claim 60, wherein said electropolished lower capacitor electrodes have a thickness of approximately 50 to 300 Angstroms.

63. (Previously presented) The capacitor structure of claim 62, wherein said lower capacitor electrodes have a thickness of approximately 100 Angstroms.

64. (Previously presented) The capacitor structure of claim 60, wherein said lower capacitor electrodes contain platinum.